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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/769,819	02/03/2004	Fusayoshi Hirotsu	08372.0017	9526

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EXAMINER	
MAI, ANH D	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 09/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/769,819	HIROTSU ET AL.	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) *21-26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 15-20* is/are rejected.

7)☒ Claim(s) *13 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/3/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I, claims 1-20 in the reply filed on August 9, 2005 is acknowledged.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 12 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The limitation of claim 12: wherein said second gate is configured to leave a portion not provided with said second gate within a region overlapping with said fist gate in a plan view, is not understood.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-12 and 15-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Arima (U.S. Patent No. 6,911,701).

With respect to claim 1, Arima teaches a semiconductor element as claimed including:

a source (2) and a drain (3);

a first gate (1) for forming a channel region of a uniform electric field between source (2) and drain (3); and

a second gate (5) for forming a channel region of a non-uniform electric field formed of strong and weak electric field regions, wherein the first (1) and second (5) gates are located between source (2) and drain (3), and overlap at least partially each other in a plan view, and

a conductance of the whole channel region between source (2) and drain (3) changes as a conductance of the channel region provided by the second gate (5) changes in accordance with a voltage applied to second gate (5). (See Figs. 11-16).

With respect to claim 2, occurrence of strong electric field region and weak electric field region of Arima partially changes a direction of the electric field in the whole channel region formed by said first (1) and second (5) gates, and the change in electric field direction modulates the effective gate length and gate width in whole channel region.

With respect to claim 3, first gate (1) of Arima has a rectangular form, and second gate (5) has a geometry defined by a group of straight lines extending along the geometry of first gate (1).

With respect to claim 4, a conductance of a whole channel region of Arima includes channels formed response by the first (1) and second (5) gates is controlled in accordance with voltages applied to first (1) and second (5) gates.

With respect to claim 5, an electric field vector in a whole channel region formed by first (1) and second (5) gates of Arima is modulated in accordance with a ratio between voltages applied to first (1) and second (5) gates, respectively.

With respect to claim 6, first (1) and second (5) gates of Arima are layered with an insulating layer interposed between first (1) and second (5) gates for electrical isolation. (See Fig. 12).

With respect to claim 7, geometry of first (1) and second (5) gates of Arima are designed such that the channel regions respectively formed by first (1) and second (5) gates between source and drain have geometrical continuity.

With respect to claim 8, in the region between source (2) and drain (3) of Arima, a first portion overlapping with first gate (1) in a plan view has an impurity concentration different from that of a second portion (51) not including first portion but overlapping with second gate (5) in a plan view. (See Fig. 12).

With respect to claim 9, in the region between source (2) and drain (3) of Arima, a first portion overlapping with first gate in a plan view has an impurity concentration substantially

equal to that of a second portion not including first portion and overlapping with second gate (5) in a plan view. (See Fig. 10 and 13).

With respect to claim 10, Arima teaches a semiconductor element as claimed including:

a source (2) and a drain (3);

a first gate (1) having a rectangular form for forming a channel region between source (2) and drain; and

a second gate (5) for forming a channel region between source (2) and drain, geometry of the second gate (5) being defined by a group of straight lines along the geometry of first gate (1), and having a gate length partially variable depending on a position along the gate width, wherein the second gate (5) is formed in a region between source (2) and drain (3), and overlaps at least partially with the first gate (1) in a plan view. (See Figs. 11-16).

With respect to claim 11, the second gate (5) of Arima, in the region between source (2) and drain (3) covers the first gate (1) in a plan view.

With respect to claim 12, as best understood by the examiner, the second gate (5) of Arima is configured to leave a portion not provided with second gate (5) within a region overlapping with the first gate (1) in a plan view. (See Fig. 11).

With respect to claim 15, a conductance of a whole channel region including channels formed response by first (1) and second (5) gates of Arima is controlled in accordance with voltages applied to first (1) and second (5) gates.

With respect to claim 16, an electric field vector in a whole channel region formed by the first (1) and second (5) gates of Arima is modulated in accordance with a ratio between voltages applied to first (1) and second (5) gates, respectively.

With respect to claim 17, the first (1) and second (5) gates of Arima are layered with an insulating layer interposed between said first (1) and second (5) gates for electrical isolation. (see Fig. 12).

With respect to claim 18, geometry of the first (1) and second (5) gates of Arima are designed such that the channel regions respectively formed by the first (1) and second (5) gates between source (2) and drain (3) have geometrical continuity.

With respect to claim 19, in the region between source (2) and drain (3) of Arima, a first portion overlapping with first gate (1) in a plan view has an impurity concentration different from that of a second portion (51) not including the first portion but overlapping with the second gate (5) in a plan view. (See Fig. 12).

With respect to claim 20, in the region between source (2) and drain (3) of Arima, a first portion overlapping with the first gate (1) in a plan view has an impurity concentration substantially equal to that of a second portion (51) not including first portion and overlapping with second gate (5) in a plan view. (See Figs. 10 and 13).

Allowable Subject Matter

5. Claims 13 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter: prior art of record fails to teaches a semiconductor element in the combination of the limitations as claimed including: second gate is not formed in a central portion, in a direction of gate width, within the region overlapping with the first gate in plan view, and is formed in a portion other than the central portion. (claim 13). Or the second gate is formed in a central portion, in a direction of gate width, within the region overlapping with the first gate in plan view, and is not formed in a portion other than the central portion. (claim 14).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (571) 272-1710. The examiner can normally be reached on 8:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH D. MAI
PRIMARY EXAMINER